CLAIMS

What is claimed is:

1. A multithreaded computer based system for enabling a command in a first thread to accessing data in a second thread comprising:

an embedded pipelined processor capable having a first program thread and a second program thread in an execution pipeline, said first program thread comprising a first set of instructions, said second program thread comprising a second set of instructions, said embedded processor comprising:

a fetch unit for fetching an instruction from program memory;

a decode unit for decoding said feteched instruction;

an execution unit for executing said decoded instructions;

a write back unit for writing the results of said executed instruction to an identified storage location;

a first set of data storage devices capable of storing a first state of said embedded processor, wherein said first state is the state of the embedded processor during the execution of the first program thread, including

a first control status register for identifying a first target set of data storage devices from which a first source operand of a first fetched instruction is to be retrieved from and for identifying a second target set of data storage

devices to which a first result of a first executed instruction is stored, wherein said first and second target set of data storage devices are different;

a second set of data storage devices capable of storing a second state of said embedded processor, wherein said second state is the state of the embedded processor during the execution of the second program thread, including:

a second control status register for identifying a third target set of data storage devices from which a second source operand of a second fetched instruction is to be retrieved from and for identifying a fourth target set of data storage devices to which a second result of a second executed instruction is stored, wherein said third and fourth target set of data storage devices are different;

a thread scheduler for identifying which of said program threads said embedded processor executes; and

an instruction set including an instruction that overwrites the first control status register when instructions associated with the first set of data storage devices are executed and overwrites the second control status register when instructions associated with the second set of data storage devices are executed;

wherein said processor switches between said first and second state in a time period between the end of the execution of a first program instruction in the first thread and the beginning of the execution of a second program instruction in the second thread;

wherein said processor switches between said first and second states by changing a state selection register.